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A thesis submitted in partial fulfilment of the requirements for the degree of BACHELOR of SCIENCE in Electrical & Electronic Engineering

Department of Electrical & Electronic Engineering
CHITTAGONG UNIVERSITY OF ENGINEERING & TECHNOLOGY

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Declaration

I hereby declare that the work contained in this Thesis has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the Thesis contains no material previously published or written by another person except where due reference is cited. Furthermore, the Thesis complies with PLAGIARISM and ACADEMIC INTEGRITY regulation of CUET.

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Dedication

To my loving parents, who have been my constant source of support, encouragement, and inspiration.

Approval by the Supervisor

This is to certify that **1st Student Name** & **2nd Student Name** has carried out this research work under my supervision, and that they have fulfilled the relevant Academic Ordinance of the Chittagong University of Engineering & Technology, so that they are qualified to submit the following Thesis in the application for the degree of BACHELOR of SCIENCE in Electrical & Electronic Engineering. Furthermore, the Thesis complies with the PLAGIARISM and ACADEMIC INTEGRITY regulation of CUET.

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Acknowledgement

First and foremost, we would like to express our gratitude to the Supreme Being, without whose blessings this thesis would not have been possible. Furthermore, we would also like to acknowledge the invaluable guidance and support provided by our supervisor, Assistant Professor [Supervisor Name], from the Department of Electrical and Electronic Engineering (EEE) at CUET.

We are also grateful to [Supervisor Name], an associate professor from the Department of Electrical and Electronic Engineering (EEE) at CUET, who has provided us with her expertise and assistance throughout the project. We also extend our heartfelt appreciation to each and every individual who has contributed to the completion of this thesis. Lastly, we would like to express our gratitude to the Department of Electrical and Electronic Engineering at CUET, Chittagong-4349, Bangladesh, for providing us with the necessary resources and facilities to undertake this research.

Abstract

A two stage CMOS 180 nm wideband (25 GHz-35 GHz) power amplifier (PA) with superimposed staggered tuning technique has been introduced in this paper. To improve the value of reflection co-efficient, gain and bandwidth ,we have implemented two stage CMOS technology rather using single stage. An input matching network and interstage matching network were designed using ADS (Advanced Design System) to improve impedance matching. The proposed PA network achieves better input matching with S_{11} values of -16.38 dB at 27.12 GHz and -10.22 dB at 32.33 GHz. The maximum value of power gain at 26.41 GHz is 27.55 dB. The average gain across the frequency range of 25 GHz to 35 GHz is 21.78 dB. At the matching frequencies of 27.12 GHz and 32.33 GHz, the gain values are 25 dB and 18.96 dB, respectively. The designed PA exhibits output return loss of less than -5 dB.

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Chapter 1

INTRODUCTION

Find the set of instructions as a standard format for the thesis report in Annex-II of this template. These guidelines provide students at CUET with essential information about preparing and submitting theses and dissertations in an acceptable format. Print those notes for future reference.

This is the first chapter of the thesis structure of the template. To craft a rewarding dissertation or Thesis, the very first thing you need to understand is dissertation structure. There are many sources that could be referred as [1], and students must learn in detail. The introduction chapter needs to state the objectives of the research program, include definitions of the key concepts and variables, and give a brief outline of the background and research approach. The aim of the introduction is to contextualize the proposed research.

In the opening paragraph, give an overall view of what is included in the chapter. For example:

This chapter outlines the background (section 1.1) and context (section 1.2) of the research and its purposes (section 1.3). Next, section 1.4 describes the significance and scope of this research and provides definitions of the terms used. Finally, section 1.5 includes an outline of the remaining chapters of the Thesis.

1.1 Background

Give background of the problem to be explored in your study and what led you to do the Thesis. For example, you might discuss educational trends related to the problem, unresolved issues, social concerns. You might also include some personal background.

1.2 CONTEXT

Outline the context of the study (i.e., the significant foci of your research) and give a statement of the problem situation (basic difficulty – areas of concern, felt need).

1.3 AIMS AND OBJECTIVES

Define the purpose and specific aims and objectives of the study. Emphasize the practical outcomes or products of the study. Delineate the research problem and outline the questions to be answered or the overarching objectives to be achieved.

1.4 SIGNIFICANCE, SCOPE AND DEFINITIONS

Discuss the importance of your research topic (problem situation), the methodology, and the gap in the literature. Outline the scope and delimitations of the study (narrowing of focus).Define and discuss terms to be used (largely conceptual here; operational definitions may follow in the Research Design chapter).

1.5 THESIS OUTLINE

[Outline the chapters for the remainder of your Thesis.] Chapter 2 reviews background literature relating ……..

……

Chapter 3 describes the procedures followed for the range of tests carried out during the project. ……..

Chapter 4 give the characterization of the materials used in the study…….

1.6 Performance Parameter

Multiple parameters were used to assess the CMOS PA's performance. The output power, power consumption, power gain, linearity, and power added efficiency (PAE) of a PA design are its most crucial components. These aspects inevitably come with trade-offs, and as a result, PA design for CMOS downscaling is difficult. These were the main criteria that were used for measuring performance.

1.6.1 Output Power

The output power (Pout) [1] is the amount of power sent to the load, which is the antenna. Higher power output must be achieved at the expense of efficiency because some power is lost as heat. To account for this power loss, the device's energy supply must be greater than its needed output power [2]. The current is essential for maintaining a consistent supply voltage and achieving the necessary output power. As a result, the output power of the power amplifier (PA), which is directly related to the PA's efficiency, determines the PA's performance. The output power is transformed into its appropriate dBm value using the following equation:

$$P_{out} = \frac{V_{out}^2}{2R_L} \tag{1.1}$$

Where V_{out} denotes the output voltage and R_L denotes the resistance load.

1.6.2 Power Consumption

The power consumption of a power amplifier (PA) is another important aspect of its performance. It's critical to address the need for extended battery life without sacrificing excessive power consumption given the rising demand for portable devices. According to the first equation, the PA's total power consumption (P_{Total}) is calculated by adding its dynamic and static power consumption. Leakage current (I_{CC}) causes static power consumption (P_S), whereas high-frequency switching causes dynamic power consumption (P_D). The two equations that follow show how to determine static and dynamic power usage. Reduced heat generation inside the device is a direct result of reduced static power, which has a major impact on overall power usage. In addition to reducing the device's exposure to heat, this decrease in power consumption increases system dependability. To extend battery life, PAs must use as little electricity as possible because excessive power utilization can reduce their longevity.

$$P_{Total} = P_S + P_D \tag{1.2}$$

$$P_S = V_{DD} \times I_{CC} \tag{1.3}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \sum \left(C_{Ln} \times f_{On}\right)\right] \tag{1.4}$$

The power consumption capacitance is denoted in the context by C_{pd} (in Farads). In Hertz, f_I stands for the input frequency, while f_{On}, also in Hertz, is the total frequency of all outputs at each output. N_{SW} stands for the total number of output switches, and V_{DD} for the supply voltage (in Volts). Additionally, the total load capacitance at each output is represented by

C_{Ln}.

1.6.3 Power Gain

Power gain (G) represents the relationship between output and input power, indicating the power amplifier's ability to deliver a significantly amplified power signal to the load [3]. It quantifies the extent to which the amplifier increases the amplitude of a signal. By enhancing the output power, a power amplifier aims to enhance efficiency and sensitivity.

$$G = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad [dB] \tag{1.5}$$

Here, P_{out} is the output power and P_{in} is the input power.

Chapter 2

LITERATURE REVIEW

2.1 Overview of CMOS Power Amplifier

A power amplifier employing complementary metal-oxide semiconductor (CMOS) technology is a type of electrical circuit. It is essential to many applications, including satellite communication, Wi-Fi, Bluetooth, and wireless communication networks like cellular networks.

In comparison to alternative amplifier technologies, CMOS power amplifiers provide a number of benefits, including high integration density, low power consumption, and compatibility with traditional CMOS processes. They are very appealing for usage in portable and low-power devices where cost effectiveness and power efficiency are crucial.

A power amplifier's main job is to boost an input signal's power level to a level appropriate for transmission or driving a load. This is accomplished in the case of CMOS power amplifiers by using CMOS transistors as the amplifying components. Input matching networks, gain stages, and output matching networks are common stages in the architecture of CMOS power amplifiers.

Power transfer is optimized by the input matching network's role in impedance matching between the amplifier and the stage before it. By doing this, it makes sure that the majority of the signal power is absorbed by the amplifier as opposed to being reflected back to the source. In addition to enhancing signal fidelity and reducing distortion, proper impedance matching.

The gain stages, which magnify the input signal to the appropriate output power level, are the heart of the power amplifier. They are made to offer high gain with a focus on linearity and low distortion. The inherent constraints of CMOS technology at high frequencies can make achieving high gain in CMOS power amplifiers difficult. Performance characteristics of the amplifier, such as power gain, bandwidth, and linearity, are influenced by parasitic capacitances and resistances in CMOS transistors.

Different design strategies are used to lessen these restrictions. The performance of the

amplifier can be enhanced through careful device sizing, layout optimization, the use of inductive components, and matching networks. To attain the needed performance at high frequencies, strategies like cascode designs, impedance modification, and distributed amplifiers are used.

In order to maximize power transfer to the load, the output matching network guarantees impedance matching between the power amplifier and the load. It is essential for effectively supplying electricity and reducing reflections that can reduce the signal quality.

A thorough understanding of circuit theory, RF (Radio Frequency) design, and CMOS device characteristics is required while designing a CMOS power amplifier. The performance of the amplifier is modeled and examined using sophisticated simulation tools and optimization techniques, taking into consideration several factors like gain, power efficiency, linearity, and bandwidth.

CMOS power amplifiers can be designed for various frequency ranges, from low-frequency applications to mm-wave frequencies. The design considerations and techniques vary depending on the targeted frequency range and application requirements. High-frequency CMOS power amplifiers often require careful consideration of the parasitic elements, transmission line effects, and the use of advanced circuit topologies and techniques.

Ongoing research and advancements in CMOS power amplifier design aim to push the boundaries of performance. Researchers are exploring novel architectures, device structures, and circuit topologies to achieve higher power efficiency, wider bandwidth, improved linearity, and integration with other circuit blocks.

In conclusion, CMOS power amplifiers provide power amplification with good efficiency, compactness, and compatibility with typical CMOS processes, making them an attractive option for integrated circuit designs. They are essential parts of contemporary wireless communication systems because they permit faster data rates, greater energy economy, and more functionality.

2.2 Existing Power Amplifier Design Techniques

CMOS technology possesses the ability to incorporate highly intricate digital circuitry, providing exceptional versatility and cost-effectiveness by integrating an entire radio system on a single chip. However, when it comes to power amplifier (PA) design, CMOS implementation poses significant challenges due to inherent limitations in standard CMOS processes from an RF perspective. These limitations include low oxide breakdown voltage, limited current drive capability, substrate coupling, and subpar quality and tolerance of on-chip passive components [4–6]. These disadvantages have a detrimental impact on PA performance,

particularly in terms of output power, efficiency, and linearity.

High-data-rate and wide-bandwidth (BW) capabilities are required due to the growing need for wideband radio frequency (RF) transceivers in radar and satellite communication systems at sub-mm wave bands. At these higher frequencies, however, constructing wideband power amplifiers (PAs) with high power added efficiency (PAE) utilizing CMOS technologies is quite difficult [7–9]. Single broadband power amplifiers (PA) that can enable ultra-high data rate modulation and concurrently amplify multiple carriers are becoming more and more necessary in contemporary communication systems. The necessity for the PA to operate over a wider bandwidth than traditional narrowband amplifiers can be found in a number of applications, including imaging systems [10].

A popular and efficient method for achieving wideband features is the use of staggered power amplifiers (PAs) [11, 12]. To achieve staggered wideband performance, this method includes designing the driver and main stages at two different center frequencies.

Chapter 3

METHODOLOGY

This chapter of the Thesis should outline the design and methodology of your research. The basis for the choice of research method should be whether it will help you answer your research question(s). Feel free to modify your chapter heading as appropriate with your research.

3.1 Lists, Flow Chart and Circuit Drawing

3.1.1 Lists

i. Determine the specifications: The initial step is to ascertain the PA's specs, such as the appropriate frequency range, output power, and gain.

ii. Select the transistor: Choose the right transistor for the amplifier based on the requirements. A CMOS transistor was used in this instance because it is appropriate for high-frequency applications.

iii. Design the first stage: The amplifier's first stage is built to deliver the appropriate gain. The stagger tuning approach should be used to build this stage, which entails changing the inductors and capacitors so that the input and output resonant frequencies are not the same. The amplifier's bandwidth is widened using this method.

iv. Design the second stage: In order to provide more gain and bandwidth, the second stage of the amplifier should likewise be developed using a stagger tuning technique.

3.1.2 Flow Chart

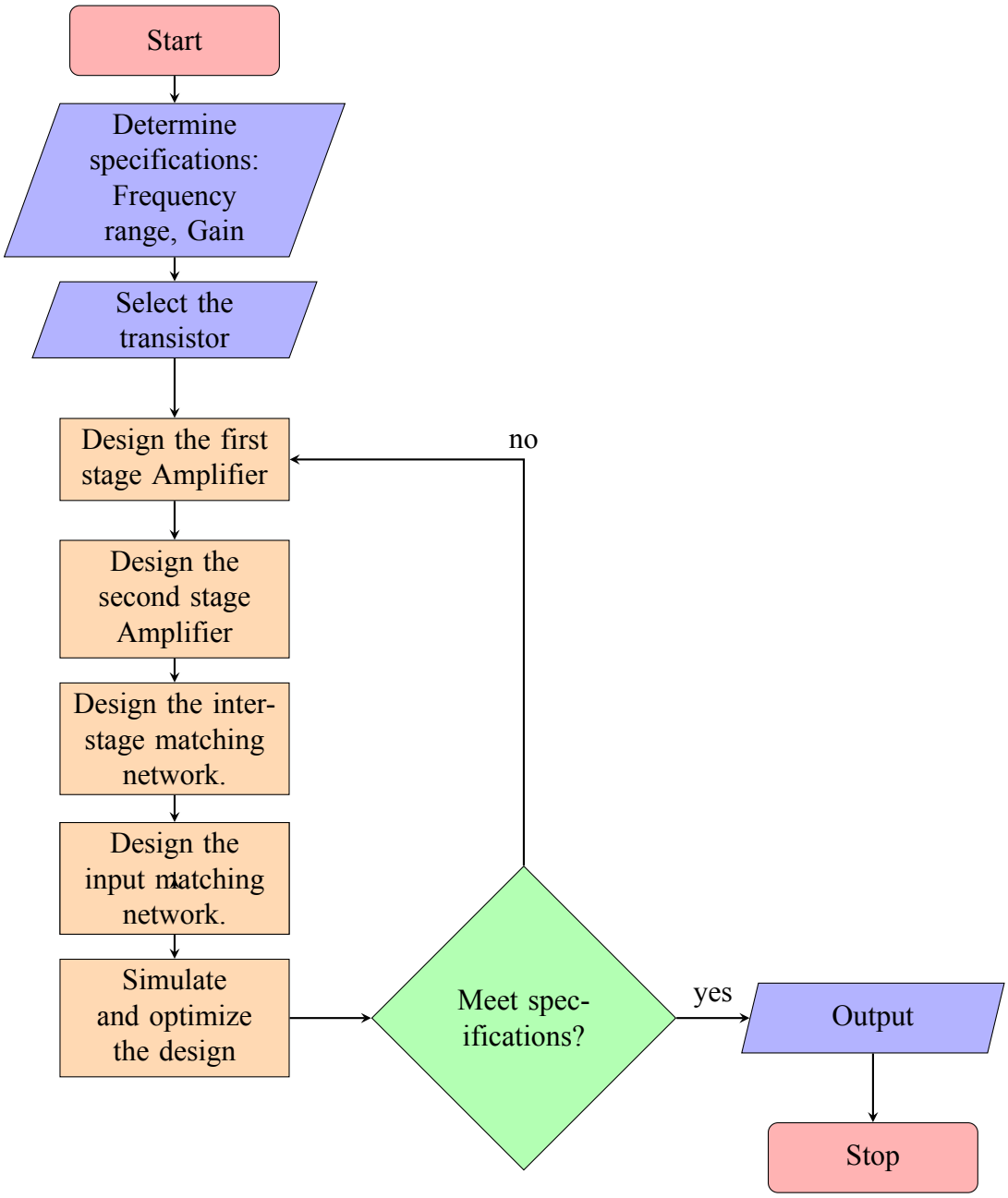

Figure 3.1: Design methodology of this work.

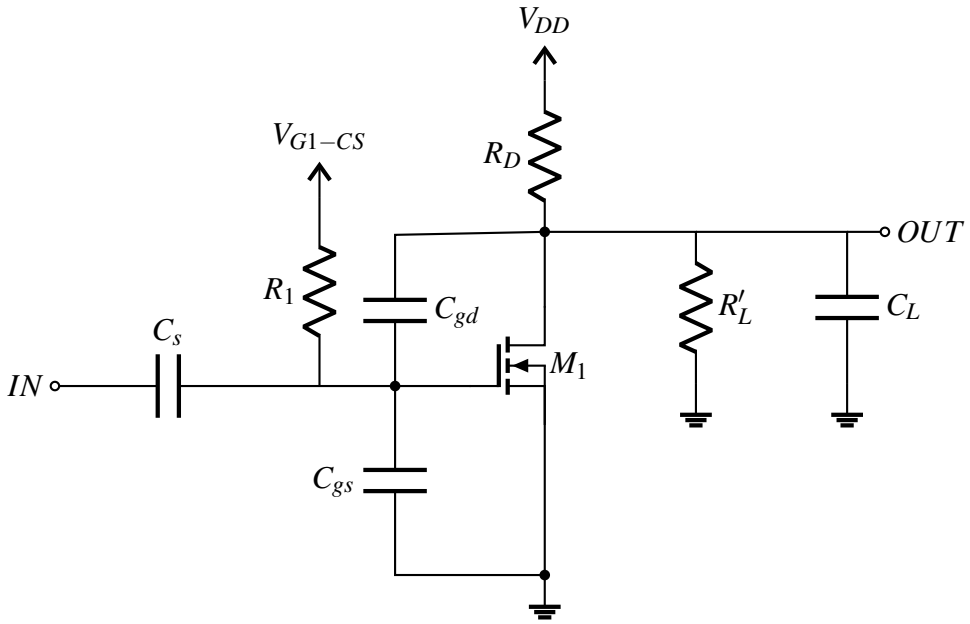

Figure 3.2: Common-source power amplifier circuit at high frequency.

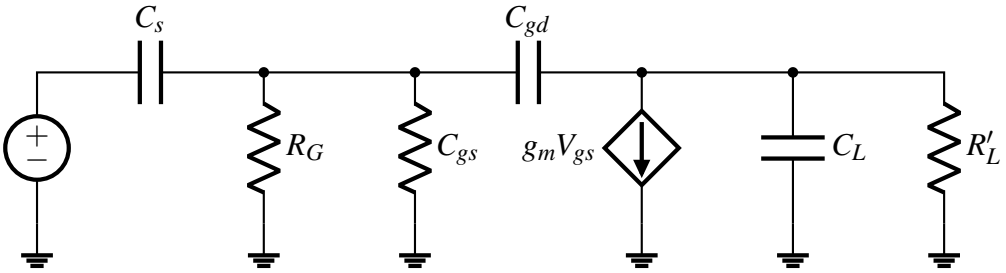

Figure 3.3: The CS power amplifier, a high frequency equivalent circuit shown in Figure 3.2.

3.1.3 Circuit Drawing

3.2 Writing Mathematical Equation

First define

$$B_{C1} = \omega C1, \quad B_{C2} = \omega C2, \quad X_L = \omega L \tag{3.1}$$

and define

$$Q_1 = B_{C1} R_1, \quad Q_2 = B_{C2} R_2 \tag{3.2}$$

$$Z_A = R_A - jX_A, \quad Z_B = R_B - jX_B \tag{3.3}$$

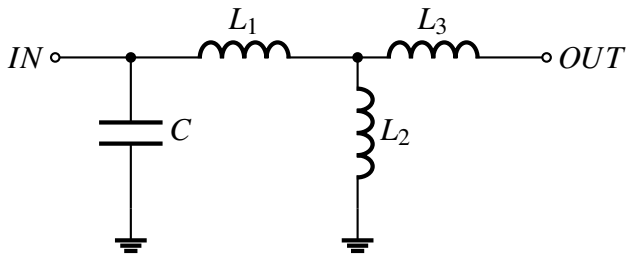

Figure 3.4: Input matching network of proposed CMOS power amplifier.

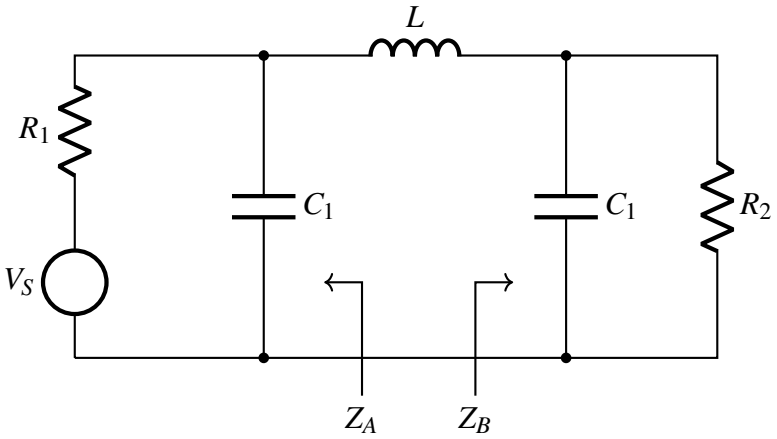

Figure 3.5: Typical circuit used for analyzing a Π-match network.

By doing basic circuit analysis

$$R_A = \frac{R_1}{1+Q_1^2}, \quad X_A = R_A Q_1 \tag{3.4}$$

$$R_B = \frac{R_2}{1+Q_2^2}, \quad X_B = R_B Q_2 \tag{3.5}$$

At conjugate match $R_A = R_B$ and $X_L = X_A + X_B$. Additionally, as the loaded Q at resonance can be represented by $Q_L = \frac{X_L}{R_A+R_B}$, the above conditions allow us to obtain the following relationships from equation (3.4) and (3.5).

$$Q_L = \frac{1}{2}(Q_1 + Q_2) \tag{3.6}$$

$$\frac{R_1}{R_2} = \frac{1+Q_1^2}{1+Q_2^2} \tag{3.7}$$

$$X_L = R_1 \frac{2Q_L}{1+Q_1^2} = R_2 \frac{2Q_L}{1+Q_2^2} \tag{3.8}$$

The condition for designing a Π-match can be derived from equations (3.6) and (3.7). An expression for Q_2 can be obtained by rearranging equation (3.7), for instance.

$$Q_2^2 = \frac{R_2}{R_1}\left(1+Q_1^2\right) - 1 \tag{3.9}$$

To ensure a positive Q_2, it is necessary to have either $R_1 > R_2$ with $Q_1 \geq \sqrt{\frac{R_1}{R_2} - 1}$, or $R_2 > R_1$ with $Q_2 \geq \sqrt{\frac{R_2}{R_1} - 1}$. Alternatively, expressed in terms of Q_L from equation (3.6), the design condition for a Π-match is that:

$$Q_L \geq \begin{cases} \frac{1}{2}\sqrt{\frac{R_1}{R_2} - 1} & \text{if } R_1 > R_2 \\ \frac{1}{2}\sqrt{\frac{R_2}{R_1} - 1} & \text{if } R_2 > R_1 \end{cases} \tag{3.10}$$

Once the condition specified in equation (3.10) is satisfied, it becomes possible to obtain the values of Q_1 and Q_2 by utilizing equations (3.6) and (3.7).

$$Q_1 = \frac{2Q_L R_1 - \sqrt{4Q_L^2 R_1 R_2 - (R_1 - R_2)^2}}{R_1 - R_2} \tag{3.11}$$

$$Q_2 = \frac{2Q_L R_2 - \sqrt{4Q_L^2 R_1 R_2 - (R_1 - R_2)^2}}{R_2 - R_1} \tag{3.12}$$

The following is the design procedure for a Π-match network:

1. Set R_1, R_2, and Q_L and check whether the condition in (3.10) is satisfied. If not, assign new values (typically to Q_L) until the condition is met.

2. After verifying that the condition in (3.10) is met, solve for Q_1 and Q_2 using (3.11) and (3.12), respectively.

3. Determine B_{C1}, B_{C2}, and X_L using equations (3.2) and (3.8).

4. Calculate C_1, C_2, and L at the frequency of interest using (3.1).

It should be noted that if one of the capacitances is set to zero, all the equations for the Π-match become equivalent to those of the L-match. This supports the idea that the L-match is a unique instance of the Π-match.

As previously mentioned, in RF power amplifier applications, R_1 and R_2 are generally selected based on power optimization, efficiency optimization, and load requirements. Thus, the subsequent discussion will concentrate on the design considerations for Q_L. Q_L determines

the matching network's bandwidth based on its definition. Thus, if the bandwidth requirement is specified,

$$Q_L \leq \frac{f_c}{BW} \tag{3.13}$$

The symbols f_c and BW refer to the center frequency and the bandwidth of the band, respectively.

With regard to out-of-band harmonic rejections, there is a trade-off in the design of Q_L for the pass-band. A lower Q_L can be used to increase bandwidth while lowering the matching network's sensitivity to changes in process, voltage, and temperature. larger Q_L values, however, are often needed for larger harmonic rejection levels. Simple network analysis can show that the value of Q_L affects the voltage transfer function of the -match network.

$$H(s) = \frac{V_2}{V_s} = \frac{R_2}{R_1 + R_2} \times \frac{1}{1 + s\left[L + (C_1 + C_2)\frac{R_1 R_2}{R_1 + R_2} + s^2 \frac{L}{R_1 + R_2}(C_1 R_1 + C_2 R_2) + s^3 L C_1 C_2 \frac{R_1 R_2}{R_1 + R_2}\right]} \tag{3.14}$$

Define ω_m as the angular frequency at the match condition, and then use (3.1), (3.2), (3.11), and (3.12) to do certain mathematical operations to arrive to

$$\omega_m C_1 = \frac{2Q_L R_1 - \sqrt{4Q_L^2 R_1 R_2 - (R_1 - R_2)^2}}{R_1 (R_1 - R_2)} \tag{3.15}$$

$$\omega_m C_2 = \frac{2Q_L R_2 - \sqrt{4Q_L^2 R_1 R_2 - (R_1 - R_2)^2}}{R_2 (R_2 - R_1)} \tag{3.16}$$

$$\omega_m L = \frac{(R_1 - R_2)^2}{2Q_L (R_1 + R_2) - 2\sqrt{4Q_L^2 R_1 R_2 - (R_1 - R_2)^2}} \tag{3.17}$$

By substituting (3.15), (3.16), and (3.17) into (3.14), where $k = R_1/R_2$, the transfer function can be expressed in terms of ω_m, Q_L, and k.In specifically, the magnitude frequency response is as follows when harmonic rejection is a concern:

$$
\begin{aligned}
|H(j\omega)| = 2&\left[(k+1)Q_L - \sqrt{4kQ_L^2-(k-1)^2}\right] \\
&\Bigg/\Bigg\{\left[2(k-1)^2Q_L - 2(k+1)\sqrt{4kQ_L^2-(k-1)^2} - 2(k-1)^2Q_L\left(\frac{\omega}{\omega_m}\right)^2\right]^2 \\
&+\Bigg(\left[3(k-1)^2 - 8kQ_L^2 + 2(k+1)Q_L\sqrt{4kQ_L^2-(k-1)^2}\right]\left(\frac{\omega}{\omega_m}\right) \\
&+\left[8kQ_L^2 - 2(k+1)Q_L\sqrt{4kQ_L^2-(k-1)^2} - (k-1)^2\right]\left(\frac{\omega}{\omega_m}\right)^3\Bigg)^2\Bigg\}^{\frac{1}{2}}
\end{aligned}
\tag{3.18}
$$

By setting the angular frequency to ω_m in equation (3.18), the magnitude response at the matching condition is obtained as

$$
|H(j\omega)| = \frac{1}{2\sqrt{k}} = \frac{1}{2}\sqrt{\frac{R_2}{R_1}} \tag{3.19}
$$

which is expected as the Π-match network is an impedance transformer. Let $S(\omega) = |H(j\omega)|\,/\,|H(j\omega_m)|$. Then, $S(\omega, Q_L, k)$ can be used to determine the lower limit of Q_L for a specified harmonic rejection, once the impedance transformation ratio k is determined. Typically, the second- and third-order harmonic rejections are specified. By substituting $\omega = 2\omega_m$ and $3\omega_m$ in the definition of $S(\omega)$ and then using equations (3.18) and (3.19), the lower limit of Q_L can be determined.

$$
\begin{aligned}
S(2\omega_m, Q_L, k) = 2\sqrt{k}&\left[(k+1)Q_L - \sqrt{4kQ_L^2-(k-1)^2}\right] \\
&\Bigg/\Bigg\{\left(\left[(k+1)^2 - 4(k-1)^2\right]Q_L - (k+1)\sqrt{4kQ_L^2-(k-1)^2}\right)^2 \\
&+\left[24kQ_L^2 - 6(k+1)Q_L\sqrt{4kQ_L^2-(k-1)^2} - (k-1)^2\right]^2\Bigg\}^{\frac{1}{2}}
\end{aligned}
\tag{3.20}
$$

$$
\begin{aligned}
S(3\omega_m, Q_L, k) = 2\sqrt{k}&\left[(k+1)Q_L - \sqrt{4kQ_L^2-(k-1)^2}\right] \\
&\Bigg/\Bigg\{\left(\left[(k+1)^2 - 18(k-1)^2\right]Q_L - (k+1)\sqrt{4kQ_L^2-(k-1)^2}\right)^2 \\
&+\left[96kQ_L^2 - 24(k+1)Q_L\sqrt{4kQ_L^2-(k-1)^2} - 9(k-1)^2\right]^2\Bigg\}^{\frac{1}{2}}
\end{aligned}
\tag{3.21}
$$

Once the desired levels of harmonic rejection are specified, we can establish the second constraint on Q_L.

$$Q_L = max\left(Q_{L,H2}, Q_{L,H3}\right) \tag{3.22}$$

The Q_L values for the second- and third-order harmonic rejections can be obtained from the graphical approach using equations (3.20) and (3.21), respectively. These Q_L values are denoted as $Q_{L,H2}$ and $Q_{L,H3}$.

The Y-parameter matrix can be defined when the losses are represented as ideal resistors in parallel with ideal inductors.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{R_{P,p}} + \frac{1}{j\omega L_p\left(1-k^2\right)} & \frac{k}{j\omega\sqrt{\left(L_pL_s\right)}\left(1-k^2\right)} \\ \frac{k}{j\omega\sqrt{\left(L_pL_s\right)}\left(1-k^2\right)} & \frac{1}{R_{P,s}} + \frac{1}{j\omega L_s\left(1-k^2\right)} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3.23}$$

Chapter 4

RESULTS

Include a paragraph at the beginning of the Results chapter outlining the structure of the chapter. The results should be reported with respect to furnishing evidence for your research question(s) as outlined in Chapter 1. Thus, you might choose to use headings that correspond to each main question of your hypothesis/objectives from Chapter 1 and/or your theoretical framework from Chapter 2.

[Chapter 4 details all the results of your study. You can put some analysis of the results here, but generally just the results are presented, without interpretation, inference, or evaluation (which will be in Chapter 5). The results should be linked inextricably to the design – describe what happened factually and unemotively. However, in certain historical, case-study and anthropological investigations, factual and interpretive material may be interwoven rather than being presented as "findings". Figure 4.1 presents typical data. Classify the results for better understanding.

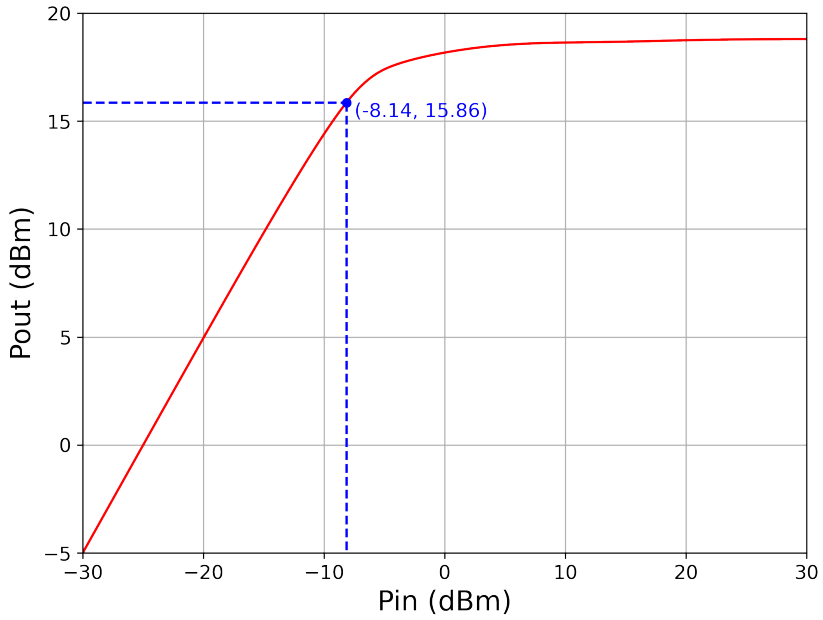

Figure 4.1: P1db compression curve of a single-stage power amplifier (shown in Figure 3.2.

You might organize your results in terms of the stages of the study (if applicable). Present the findings/results in tables or charts when appropriate, making sure to use correct formatting for any tables used. Your results must be clear, concise, focused, structured and backed up by evidence from the experiment. Present your findings in the table and a chart/figure. Describe in detail by explaining the findings. Explore the significance of the results.]

Chapter 5

ANALYSIS/DISCUSSION

As with the previous chapters, include a paragraph at the beginning summarising the structure of the chapter. Organize the chapter in terms of the objectives of the study and/or the theoretical framework. For each objective, discuss the results with reference to the literature, for example, the similarities/differences to the findings in the literature review. Develop theory or models from this comparison and evaluation.

5.1 General

[Chapter 5 contains a full discussion, interpretation, and evaluation of the results with reference to the literature. This chapter can also include theory building. However, some supervisor may want you to combine chapters 4 and 5, so that you both present and interpret the meaning of the data at the same time. Check with your Supervisor what their preference. Details can be checked from It can be useful to check your literature and try to find a place for as much of the literature as you can. If you find that a section of your literature can not be used in this chapter, it may be useful to consider the pertinence of this literature and reduce the space in the literature chapter given to it.

5.2 Performance Comparison Table

Table 5.1: Performance comparison with the wideband PA.

Ref.	CMOS Tech.	Gain (dB)	Freq (GHz)	P_{1dB} (dBm)	P_{sat} (dBm)	FBW (GHz)
This Work	90 nm	25	27.12	15.86	12	(20.1%) (25.66-31.1)
[13]	180 nm	12.0	18	12.3	16.6	(44.44%) (14-22)
[14]	180 nm	16.3	22	14.3	16.8	(18.2%) (20-24)
[15]	180 nm	15.2	26	16	19.5	(58.8%) (18-33)
[16]	65 nm	20.6	15.5	11.6	13.9	(33.8%) (13.5-19)
[17]	28 nm	15.7	30	13.2	14	(13.2%) (27.4-32.2)
[18]	28 nm	21.2	24	18.2	19.7	(31.7%) (21.8-30)

Chapter 6

CONCLUSION

[This chapter summarizes the contents discussed in the introduction, methodology, results, and discussion section without repetition. It contains general, key findings, conclusions, limitations, implication issues and future recommendations – so what is the theory? Where to from here? What are the practical implications? Discussion of where the study may be extended. The purpose of this chapter is not just to reiterate what you found but rather to discuss what your findings mean in relation to the theoretical body of knowledge on the topic and your profession. Typically, students skimp on this chapter even though it may be the most important one because it answers the ”So what?” question. Begin by discussing your findings in relation to the theoretical framework introduced in the literature review.]

6.1 General

The conclusion is an opportunity to remind the reader why you took the approach you did, what you expected to find, and how well the results matched your expectations. To avoid repetition, instead of just writing a summary of each chapter, you can write more reflectively here. You might consider how effective your methodology was in answering your research questions, and whether any new questions or unexpected insights arose in the process.The opening section(s) of the chapter should be a brief summary of everything covered so far. Follow this with your conclusions. This is the “so what” of the findings – often the hypothesis/research question(s) restated as inferences with some degree of definitive commitment and generalisability, and the raising of new and pertinent questions for future research. You could include a final model of the theory. It can be useful to use the purposes from Chapter 1 as an organizing structure for this chapter. The chapter should also include a discussion of any limitations of the research and should end with your final recommendations – practical suggestions for implementation of the findings/outcomes or for additional research.

6.2 KEY FINDINGS

Add sub-section(s), if necessary

6.3 LIMITATION OF THE STUDY

This section outlines the limitations of the study.

6.4 PRACTICAL IMPLICATION [FEEL FREE TO MODIFY

Provide the suggested implementation of your research. This may include institutional support, marketing policy etc.

6.5 RECOMMENDATION FOR FURTHER STUDY

Obviously, the Thesis or dissertation ends with a brief conclusion that provides closure. A strong final sentence should be written.

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